REMARKS

Claims 1-9, 21, and 23 are pending. Claims 1-9, 21, and 23 stand rejected. In this response, no claim has been canceled or amended. Reconsideration of the present application is respectfully requested.

Claims 1-9, 21, and 23 are rejected under 35 U.S.C. §112, first paragraph. The Examiner objected to the limitation of a wait control logic that signals a processor to indicate that the requested data is ready to be read on a next processor cycle if the requested data is in the cache memory. The Examiner stated that the above limitation is not supported in the description.

Applicant respectfully disagrees. Applicant respectfully submits that the above limitation is fully supported and described throughout the specification. Specifically, the specification states:

> "If there is a cache miss, i.e., if the comparison determines that the latched address is not stored in address cache 44, the quadword address can then be stored in counter 42, where it is used to select the first designated quadword in array 33, and can later be used to increment the address for subsequent quadwords in a burst transfer. A signal from comparator 40 can also be sent to wait control logic 49, which asserts the WAIT# signal at this time to tell the CPU that it will have to wait until the requested read data is available. Once the requested address in array 33 has been accessed, the outputs of the 64 memory cells at the designated quadword address can then be latched in latch 46, which in turn outputs the data to data cache 45 and presents the same data to multiplexer 48. At this time, array 33 can also send a signal to wait control logic 49 to deassert the WAIT# signal, as the requested data will be available on the next clock cycle. Data cache 45 stores the data that was retrieved from array 33, while the associated address is also stored in address cache 44. Address cache 44 and data cache 45 therefore combine to store the data and associated addresses that are held in cache memory at any given time."

(Specification, paragraph 21 of pages 6-7, emphasis added).

Thus, the claimed limitations are fully supported and described in the specification. Withdrawal of the rejections is respectfully requested.

Claims 1-9 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,263,398 of Taylor et al. ("Taylor"). Applicant respectfully submits that claims 1-9, 21, and 23

include limitations that are not disclosed by Taylor. In particular, independent claim 1 includes a memory device that includes a wait control logic coupled to a processor, a main memory, and a cache memory, where the wait control logic signals the processor, if data currently requested is not in the cache memory, to indicate that the requested data is not ready to be read, and the wait control logic signals the processor to indicate that the requested data is ready to be read on a next processor cycle, if the requested data is in the cache memory. These limitations are absent from Taylor.

In the Office Action, the Examiner stated:

> "AS to claims 1 and 6, Taylor discloses the recited memory device integrated with cache (see Abstract, Figure 1, and column 3 lines 7-35), and stores recently accessed data at 14 and associated addresses at 24. Taylor also additionally teaches the recited wait control signal to the extent disclosed (see 37 CFR 112 rejection above), see signal READY 32 in Fig. 1, and described at col. 5 lines 19-24 and 56-62."

(11/17/2003 Office Action, page 3, emphasis added).

Applicant respectfully disagrees. Figure 1 and its corresponding of Taylor description fail to disclose a wait control logic as claimed in the present application. In order to anticipate claim 1, Taylor has to disclose every limitations as claimed in claim 1. Since there is no wait control logic disclosed by Taylor, Taylor cannot anticipate claim 1.

Even if, for the sake of the argument, the READY signal of Taylor implicated a wait control logic, Taylor still fails to disclose a wait control logic that is coupled to a processor, a main memory, a cache memory. Furthermore, most importantly, Taylor fails to disclose a wait control logic that signals the processor to indicate that the requested data is not ready to be read if the data currently requested is not in the cache memory, and signals the processor to indicate that the requested data is ready to be read on a next processor cycle if the requested data is in the cache memory. Therefore, independent claim 1 is not anticipated by Taylor.

Independent claim 6 includes limitations similar to those referred by claim 1. Therefore for reasons similar to those discussed above, claim 6 is not anticipated by Taylor.

Given that claims 2-5, 7-9, 21, and 23 depend from one of the above independent claims, it is respectfully submitted that claims 2-5, 7-9, 21, and 23 are also not anticipated by Taylor. Withdrawal of the rejections is respectfully requested.

With respect to claims 2 and 7, claims 2 and 7 include an address latch logic to receive the addresses of the requested data, an address cache memory coupled to the address latch logic and the wait control logic to store the addresses, and a data cache memory coupled to the address cache memory and the main memory to store the data. Applicant respectfully submits that the above limitations are absent from Taylor. The Examiner contends that Figure 1 of Taylor reads on the above limitations. Specifically, the Examiner stated:

> "As to claims 2-4 and 7-9, Taylor discloses address latch logic 18, 20, address cache and comparison at 24, and data cache 14. See Fig. 1, and col. 4, lines 56-66, and col. 5, lines 60-62."

(11/17/2003 Office Action, page 3, emphasis added).

Applicant respectfully disagrees. There is no address cache memory shown in Figure 1 of Taylor. The compare block 24 does not include an address cache, particularly, an address cache memory coupled to the address latched logic and the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched.

Even if, for the sake of the argument, the compare block 24 included an address cache memory, Taylor still fails to disclose an address cache memory that is coupled to the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched. Taylor still fails to disclose a data cache memory

coupled to the address cache memory and the main memory to store the recently accessed data, where the data cache memory receives data from the main memory if the data requested is not in the data cache memory.

With respect to claims 3 and 8, claims 3 and 8 include a comparator coupled to the address latch logic and the address cache memory, where an output of the comparator is coupled to the wait control logic to cause the wait control logic to assert a signal to the processor if the address stored in the address latch logic is not found in the address cache memory. Applicant respectfully submits that these limitations are also absent from Taylor.

The Examiner contends that compare block 24 of Taylor reads on the above limitations. Applicant respectfully disagrees. There is no showing or suggestion that compare block 24 includes a comparator and an address cache memory in Taylor. Even if, for the sake of the argument, the compare block 24 might include a comparator and an address cache memory, Taylor still fails to disclose or suggest an output of the comparator coupled to the wait control logic to cause the wait control logic to assert a signal to the processor if the address stored in the address latch logic is not found in the address cache memory.

With respect to claims 4 and 9, claims 4 and 9 include limitations that the comparator causes the wait control logic to assert a signal having one cycle to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the address of the requested data is found in the data cache memory. Applicant respectfully submits that these limitations are also absent from Taylor.

The Examiner contends that Figure 4 of Taylor reads on the above limitations referred by claims 4 and 9. Applicant respectfully disagrees. Figures 4A and 4B of Taylor are flow diagrams illustrating a process or processes. Applicant respectfully submits that Figures 4A and 4B fail to disclose or suggest a comparator causes the wait control logic to assert a signal having

one cycle to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the address of the requested data is found in the data cache memory.

Claims 1-9, 21, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,288,923 of Sakamoto ("Sakamoto") in view of the alleged admitted prior art. Applicant respectfully submits that neither Sakamoto nor the alleged admitted prior art, individually or in combination, discloses or suggests the above discussed limitations. Therefore, at least for the reasons similar to those discussed above, claims 1-9, 21, and 23 are patentable over Sakamoto in view of the alleged admitted prior art. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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